What is claimed is:

1. A ESD protection device comprising:

a) a n-doped region and a p-doped region in a p-well in a semiconductor structure; said n-doped region and said p-doped region are spaced;

b) a n-well and a deep n-well surrounding said p-well on the sides and bottom;

c) a first I/O pad connected to said n-doped region;

d) a trigger circuit connected said first I/O pad and said p-doped region;

e) a second I/O pad connected to said n-well;

f) a parasitic bipolar transistor is comprised of the n-doped region functioning as a collector terminal, the P-well functioning as a base terminal, and the deep N-well functioning as the emitter terminal; whereby under an ESD condition, the p-well is charged positive using the trigger circuit and said parasitic bipolar transistor can be turned on.

2. The ESD protection device of claim 1 which further comprises:

a first gate over said p-well between said n-doped region and said p-doped region; and

a second gate over said p-well between said p-doped region and said n-well.

3. The ESD protection device of claim 1 which further comprises:

a first gate over said p-well between said n-doped region and said p-doped region; and

a second gate over said p-well between said p-doped region and said n-well;

said second I/O pad connected to said first gate and said second gate.

4. The ESD protection device of claim 1 which further comprises said n-doped region and said p-doped region are separated by an isolation region.

5. The ESD protection device of claim 1 wherein said trigger circuit comprises a chain of diodes.

6. The ESD protection device of claim 1 wherein said trigger circuit comprises a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor connected to said second I/O pad.

7. The ESD protection device of claim 1 wherein said trigger circuit comprises a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor connected to said second I/O pad; said RC network has a RC time constant about 10 times the duration of human body model ESD waveform.

8. The ESD protection device of claim 1 wherein said trigger circuit comprises a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor

connected to said second I/O pad; said RC network has a RC time constant between about 1.5 and 2 micro seconds.

9. The ESD protection device of claim 1 wherein said trigger circuit comprises a grounded–gate nMOS transistor and a resistor connected to the grounded–gate nMOS transistor and to said second I/O pad.

10. The ESD protection device of claim 1 which further includes a N-doped ring region laterally surrounding said p-doped region whereby said N-doped ring region and said deep n-well increase the resistance of the parasitic bipolar transistor thereby increasing the pinch off during an ESD event.

11. The ESD protection device of claim 1 wherein said semiconductor structure is comprised of silicon.

12. The ESD protection device of claim 1 wherein contacts to said n-doped and said p-doped regions are comprised of a silicide.

13. The ESD protection device of claim 1 wherein said ESD protection device is further comprised of a second parasitic bipolar transistor.

14. A method of forming an ESD protection device comprising:

a) forming a n-doped region and a p-doped region in a p-well in a semiconductor structure; said n-doped region and said p-doped region are spaced;

b) forming a n-well and a deep n-well that surround said p-well on the sides and bottom;

c) connecting electrically a first I/O pad to said n-doped region;

d) connecting electrically a trigger circuit said first I/O pad and said p-doped region;

e) connecting electrically a second I/O pad to said n-well; whereby a parasitic bipolar transistor is comprised of the n-doped region functioning as a collector terminal, the P-well functioning as a base terminal, and the deep N-well functioning as the emitter terminal; whereby under an ESD condition, the p-well is charged positive using the trigger circuit and the parasitic bipolar transistor can be turned on.

15. The method of claim 14 which further comprises;

forming a first gate over said p-well between said n-doped region and said p-doped region; and

forming a second gate over said p-well between said p-doped region and said n-well;

electrically connecting said first gate, said second gate and second I/O pad.

16. The method of claim 14 which further comprises:

forming a first gate over said p-well between said n-doped region and said p-doped region; and

forming a second gate over said p-well between said p-doped region and said n-well.

17. The method of claim 14 which further includes forming isolation regions separating said n-doped region and p-doped region.

18. The method of claim 14 wherein said trigger circuit is formed by forming a chain of diodes.

19. The method of claim 14 which further includes forming said trigger circuit by forming a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor connected to said second I/O pad.

20. The method of claim 14 which further includes forming said trigger circuit by forming a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor connected to said second I/O pad; said RC network has a RC time constant about 10 times the duration of Human body model (HBM) ESD waveform.

21. The method of claim 14 which further includes forming said trigger circuit by forming a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor connected to said second I/O pad; said RC network has a RC time constant between about 1.5 and 2 micro seconds.

22. The method of claim 14 which further includes forming said trigger circuit by forming a grounded–gate nMOS transistor and a resistor connected to the grounded–gate nMOS transistor and to the second I/O pad.

23. The method of claim 14 which further includes forming a N-doped ring region laterally surrounding said p-doped region whereby said N-doped ring region and said deep n-well increase the resistance of the parasitic bipolar transistor thereby increasing the pinch off during an ESD event.

24. The method of claim 14 wherein said semiconductor structures comprised of silicon.

25. The method of claim 14 which further includes forming contacts comprised of a silicide to the n-doped regions and said p-doped regions.

26. A method for using an ESD protection device comprising the steps of:

(1) providing:

a) a n-doped region and a p-doped region in a p-well in a semiconductor structure; said n-doped region and said p-doped region are spaced;

b) a n-well and a deep n-well surrounding said p-well on the sides and bottom;

c) a first I/O pad connected to said n-doped region;

d) a trigger circuit connected said first I/O pad and said p-doped region;

e) a second I/O pad connected to said n-well;

f) a parasitic bipolar transistor is comprised of the n-doped region functioning as a collector terminal, the P-well functioning as a base terminal, and the deep N-well functioning as the emitter terminal;

(2) charging said p-well using the trigger circuit under an ESD condition and turning on said parasitic bipolar transistor.

27. The method of claim 26 which further comprises:

forming a first gate over said p-well between said n-doped region and said p-doped region; and

forming a second gate over said p-well between said p-doped region and said n-well.

28. The method of claim 26 which further comprises;

forming a first gate over said p-well between said n-doped region and said p-doped region; and

forming a second gate over said p-well between said p-doped region and said n-well;

connecting said second I/O pad to said first gate and said second gate.

29. The method of claim 26 wherein said trigger circuit is comprised of a chain of diodes.

30. The method of claim 26 wherein said trigger circuit comprises a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor connected to said second I/O pad.

31. The method of claim 26 wherein said trigger circuit comprises a grounded–gate nMOS transistor and a resistor connected to the grounded–gate nMOS transistor and to said second I/O pad.

32. The method of claim 26 which further includes forming a N-doped ring region laterally surrounding said p-doped region whereby said N-doped ring region and said deep n-well increase the resistance of the parasitic bipolar transistor thereby increasing the pinch off during an ESD event.

33. A method of using a ESD protection device comprising the steps of :

(1) providing:

a) a n-doped region and a p-doped region in a p-well in a semiconductor structure; said n-doped region and said p-doped region are spaced;

b) a n-well and a deep n-well surrounding said p-well on the sides and bottom;

c) a first I/O pad connected to said n-doped region;

d) a trigger circuit connected said first I/O pad and said p-doped region;

e) a second I/O pad connected to said n-well;

f) a parasitic bipolar transistor is comprised of the n-doped region functioning as a collector terminal, the P-well functioning as a base terminal, and the deep N-well functioning as the emitter terminal; whereby under an ESD condition, the p-well is charged positive using the trigger circuit and said parasitic bipolar transistor can be turned on;

g) a N-doped ring region laterally surrounding said p-doped region whereby said N-doped ring region and said deep n-well increase the resistance of the parasitic bipolar transistor thereby increasing the pinch off during an ESD event;

(2) reverse-biasing said N-doped ring region during an ESD event to increase the effective resistance seen by the injected current in the P-doped region by said trigger circuit into p-well.